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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/242,974	02/26/1999	MICHEL UGON	T2146-906088	1762

181 7590 11/16/2004

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/242,974	UGON, MICHEL	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-39 and 41-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-39 and 41-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20-39 and 41-50 have been considered. Claims 20, 23-39 and 41-50 have been amended as per Applicant's requests.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 20-37, 39, and 41-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin, U.S. Patent Number 5,361,337 (herein referred to as Okin) in view of Fletcher et al., U.S. Patent Number 5,012,409 (herein referred to as Fletcher) and further in view of Griffin, III et al., U.S. Patent Number 5,249,294 (herein referred to as Griffin).

4. Referring to claim 20, Okin has taught an unpredictable microprocessor or microcomputer comprising:

a. A main memory including a main program (Okin column 2, lines 8-20) and a secondary program (Okin column 2, lines 8-20), wherein said secondary program is not related to the main program (Okin column 2, lines 8-20). In regards to Okin, it is inherent that the main program and secondary program are unrelated, since a context switch is only necessary to save the state of a current process when a completely different process, with different state information, is to be run.

b. A first RAM-type working memory (Okin column 1, lines 17-24; column 3, lines 62-64; column 4, lines 6-26; Figure 3B; and Figure 4);

c. A second RAM-type working memory (Okin column 1, lines 17-24; column 3, lines 62-64; column 4, lines 6-26; Figure 3B; and Figure 4);

d. A processor adapted to execute instructions from one or more of said main memory, said first working memory, and said second working memory (Okin column 1, lines 17-24 and column 3, lines 1-25);

e. A bus connecting the processor to the main memory, the first working memory and the second working memory (Okin column 4, lines 28-50 and 59-61 and Figure 3A). In regards to Okin, it is inherent that the local bus in Figure 3A is connected to the main memory, first working memory, and second working memory, since the device fetches instructions and data from these memories.

f. Switching means for switching while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories (Okin column 3, lines 36-44), said switching means comprising:

i. Access registers associated with each of the main memory, the first working memory, and the second working memory (Okin column 3, lines 62-64; column 4, lines 7-12; Figure 3B; and Figure 4);

ii. At least one first block of registers that stores the operating context of the programs in the main memory (Okin column 4, lines 12-26 and Figure 4); and

iii. A switching circuit that enables one of the working memories and controls the access registers associated with each of the main memory, the first

working memory and the second working memory (Okin column 4, lines 4-26 and Figure 4).

5. Okin has not taught the main memory contains an operating system. Fletcher has taught the main memory contains an operating system (Fletcher column 1, lines 16-18). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the operating system in main memory coordinates processes. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the operating system in main memory, of Fletcher, in the device of Okin to coordinate processes.

6. In addition, Okin has not taught unpredictably jumping. Griffin has taught unpredictable jumping (Griffin columns 1-2, lines 58-11). In regards to Griffin, the interrupts are inherent in order to jump to the interim routines in the middle of a process. A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

7. Referring to claim 21, Okin has taught the microprocessor or microcomputer further comprising a second block of registers for storing the operating context of the secondary program (Okin column 4, lines 12-26 and Figure 4).

8. Referring to claim 22, Okin has not taught the microprocessor further including means for de-correlating the running of the programs from an isochronous clock. Griffin has taught

means for de-correlating the running of the programs from an isochronous clock (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

9. Referring to claim 23, Okin has not taught wherein the main program can enable or inhibit the switching means by loading the switching circuit to switch and enable the working memories and the first block and second block of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program. Fletcher has taught the main program can enable or inhibit the switching means by loading the switching circuit for switching and enabling the working memories and the first block and second block of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program (Fletcher column 1, lines 16-20 and 33-44). In regards to Fletcher, the program, or task, is written from instructions made available and understood by the operating system. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the main program controls the processor's function. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the main program of Fletcher for control over the processor.

10. Referring to claim 24, Okin has not taught wherein the second working memory and its access registers are substituted for the working memory and its access registers in utilization by a main program. Fletcher has taught the second working memory and its access registers are substituted for the working memory and its access registers in utilization by a main program (Fletcher column 1, lines 16-20 and 36-44). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the above controls the generating and switching of processes and its resources. Therefore it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the above, as taught by Fletcher, in the device of Okin.

11. Referring to claim 25, Okin has not taught wherein the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, the random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program. Griffin has taught the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, the random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the random number generator is inherent in order to determine the random duration interval and the interrupt circuit and interrupt are inherent in order to jump to the interim routines in the middle of a process. A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported in Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have

been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

12. Referring to claim 26, Okin has not taught means for de-correlating the running of the programs from an isochronous clock, wherein the de-correlating means comprises a time counting system independent from the processor that, after the time count, triggers an interrupt for returning from the secondary program to the main program. Griffin has taught means for de-correlating the running of the programs from an isochronous clock, characterized in that the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the clock system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermined process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating as taught by Griffin provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

13. Referring to claim 27, Okin has not taught means for de-correlating the running of the programs from an isochronous clock, wherein the switching means is controlled by the processor and its program, by de-correlating means, by a timer, or by any combination of at least two of the three named elements. Griffin has taught means for de-correlating the running of the programs from an isochronous clock, characterized in that the switching means is controlled by the

processor and its program, by de-correlating means, by a timer, or by any combination of at least two of the three named elements (Griffin columns 1-2, lines 58-11). In regards to Griffin, the clock system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermined process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating as taught by Griffin provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

14. Referring to claim 28, Okin has not taught wherein the switching means is enabled by being loaded by the processor running a sequence in the main program sequence. Fletcher has taught the switching means is enabled by being loaded by the processor running a sequence in the main program sequence (Fletcher column 1, lines 16-20 and 36-44). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for switching controls the processor's function. Therefore, It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the means for switching as taught by Fletcher in the device of Okin.

15. Referring to claim 29, Okin has taught wherein the secondary program uses a working space identical to that of the main program in the main memory (Okin column 2, lines 8-20). It is implied that the working space is identical, since they use the same cache.

16. Referring to claim 30, Okin has taught wherein the secondary program uses a working space smaller than that of the main program (Okin column 2, lines 8-20). It is inherent that the working space is smaller, since it uses the same cache as the main program.

17. Referring to claim 31, Okin has taught wherein the switching means carry out the substitution of the memories and the associated contexts within the execution cycle of the instruction from the microprocessor (Okin column 4, lines 13-20).

18. Referring to claim 32, Okin has taught wherein the secondary program does not modify general operating context of the main program in order to allow the main program to return without having the reestablish said context (Okin column 4, lines 4-26 and 44-48).

19. Referring to claim 33, Okin has taught wherein the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program (Okin column 4, lines 4-26 and Figure 4).

20. Referring to claim 34, Okin has taught means for substituting the memory of the secondary program for the memory of the main program (Okin column 4, lines 4-26). It is inherent since the main program can choose where to read and write.

21. Referring to claim 35, Okin has taught wherein the main program can use the first working memory and the second working memory alternately or simultaneously (Okin column 4, lines 4-26). It is inherent since the main program can choose where to read and write.

22. Referring to claim 36, Okin has taught wherein loading of the switching circuit makes it possible to mask or unmask de-correlating interrupts (Okin column 4, lines 4-26). It is inherent to be able to mask or unmask interrupts, because the switching means needs to be able to identify and use interrupts when they occur, randomly or not.

23. Referring to claim 37, Okin has taught that wherein an interrupt triggered by the secondary program effects return to the main program after the switching register has been properly loaded, by executing an instruction of the main program or the secondary program, in order to unmask the interrupts (Okin column 4, lines 4-36). It is inherent that, while the interrupt is being processed, the pipeline will continue until the interrupt is decoded.

24. Referring to claim 39, Okin has not taught the microprocessor further including means of de-correlating the run-through of the programs with respect to an isochronal clock. Griffin has taught means of de-correlating the run-through of the programs with respect to an isochronal clock (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

25. Referring to claim 41, Okin has taught wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory (Okin column 4, lines 4-26 and Figure 4).

26. Referring to claim 42, Okin has not taught wherein the de-correlating means comprise a random generator. Griffin has taught the de-correlating means comprise a random generator (Griffin columns 1-2, lines 58-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for

de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

27. Referring to claim 43, Okin has not taught wherein the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, an interruption trigger to return from the secondary program to the main program. Griffin has taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, an interruption trigger to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

28. Referring to claim 44, Okin has taught wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or a combination of at least two out of the three named elements (Okin column 3, lines 28-44).

29. Referring to claim 45, Okin has not taught wherein the main program is adapted to enable or inhibit the switching means by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory. Fletcher has taught the main program is adapted to enable or inhibit the switching means by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory (Fletcher column 1, lines 16-20 and 36-44). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the main program controls the processor's function, which includes the switching mechanism. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the main program as taught by Fletcher in the device of Okin.

30. Referring to claim 46, Okin has taught wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by the main program, with said first working memory and the associated access registers of the first working memory (Okin column 4, lines 4-26 and Figure 4).

31. Referring to claim 47, Okin has taught wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or by a combination of at least two out of the three named elements (Okin column 3, lines 28-44).

32. Referring to claim 48, Okin has not taught wherein the interrupt circuit triggers the random number generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program. Griffin has

taught the interrupt circuit triggers the random number generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made, as supported by Griffin, would have recognized that incorporating the interruption circuit prevents "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate interruption circuit as taught by Griffin in the device of Okin to improve security.

33. Referring to claim 49, Okin has taught the switching means is controlled by one of the microprocessors and the program thereof, the random interruption system, a time counter or by a combination of at least two of the three named elements (Okin column 3, lines 28-44). It is inherent that an interrupt can only occur when an interrupt is introduced by a source. Okin has not taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program. Griffin has taught the de-correlating means include a time counting system independent from the processor for enabling, at the end of a time count, the triggering of the random interrupt to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating provides a way to return to the main program to complete the processor's task. Therefore, it

would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

34. Referring to claim 50, Okin has taught wherein the switching means is confirmed by loading from the processor executing a main program sequence (Okin column 4, lines 4-26 and Figure 4).

35. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okin in view of Fletcher and in further view of Griffin, as applied to claim 20 above, and further in view of Takagi, U.S. Patent Number 5,280,618 (herein referred to as Takagi). Okin has not taught wherein the microcomputer or microprocessor is embodied in a monolithic integrated circuit. Takagi has taught the microcomputer or microprocessor is embodied in a monolithic integrated circuit (Takagi column 1, 14-22). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the monolithic integrated circuit of Takagi broadens the number of applications the computer or processor may be used for. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the monolithic integrated circuit of Takagi in the device of Okin to increase usefulness.

Response to Arguments

36. Applicant argues, in essence, "...it is readily apparent that the structural features recited in Claim 20 are neither taught nor suggested by the references of record." This has not been found persuasive. A detailed mapping of the claim limitations with the cited patents is found in the table below.

Claim 20 Limitation	Prior Art citation and explanation

A main memory including an operating system	Fletcher column 1, lines 16-18: Fletcher describes the reasons for having an OS in the lines cited.
A main memory including a main program and a secondary program	Okin column 2, lines 8-20: Okin describes switching the state of the processor on a cache miss from the first process to a second process. He also explicitly states on lines 18-20 that the number of processes does not matter. The claim recites, in the broadest interpretation possible, simply multiple processes. The labels "main program" and "secondary program" do not distinguish between a first and second process. The first process in Okin is the main program and the second process is the secondary program or vice versa.
Wherein said secondary program is not related to the main program	Okin column 2, lines 8-20: It is inherent that the main program and secondary program are unrelated, since a context switch is only necessary to save the state of a current process when a completely different process, with different state

	information, is to be run. Also, if the processes were related, it would not be possible for the second process to run with the first process waiting for a cache miss to resolve, since the data and result of the first processes instructions is not available.
A first RAM-type working memory; A second RAM-type working memory	Okin column 1, lines 17-24; column 3, lines 62-64; column 4, lines 6-26; Figure 3B; and Figure 4: As can be seen in Figure 3B and Figure 4 and explained in the corresponding lines cited, there is a write-read buffer placed between main memory and the register file to store most recently used and common instructions. As shown in Figure 4, when there are multiple processes, there are multiple write-read buffers related to each individual process. RAM type memory is a type of buffer. Please see the provided definitions for more information regarding RAM and buffer.
A processor adapted to execute instructions from one or more of said main memory, said	Okin column 1, lines 17-24 and column 3, lines 1-25:

first working memory, and said second working memory	As stated in column 3, lines 21-25, the pipeline of a processor includes an execution stage where the current instruction, which comes from one of the processes in main memory, is executed.
A bus connecting the processor to the main memory, the first working memory and the second working memory	Okin column 4, lines 28-50 and 59-61 and Figure 3A: It is inherent that the local bus in Figure 3A is connected to the main memory, first working memory, and second working memory, since the device fetches instructions and data from these memories.
Switching means for switching while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories	Okin column 3, lines 36-44: As stated in these lines from Okin, the processor switches from the first process to a second process, and saves the state of the current process before switching.
Access registers associated with each of the main memory, the first working memory, and the second working memory	Okin column 3, lines 62-64; column 4, lines 7-12; Figure 3; and Figure 4: As shown in Figures 3B and 4, the working memories feed into register files. Figure 3A shows that main memory feeds into a pre-fetch

	queue, which can be a RAM type memory. Please see the attached definitions for more information.
At least one first block of registers that stores the operating context of the programs in the main memory	Okin column 4, lines 12-26 and Figure 4: As stated in the lines cited from Okin and in Figure 4, the condition codes and other registers fed into by the ALSU preserves the context of the current process, i.e. it saves and stores the operating context of the current program. These registers in turn feed out to main memory during the write result stage of the pipeline.
A switching circuit that enables one of the working memories and controls the access registers associated with each of the main memory, the first working memory and the second working memory	Okin column 4, lines 4-26 and Figure 4: The switching circuit is the MUX which feeds selects which write-read buffer to read data from and which register file to store that data to.
Unpredictable jumping	Griffin columns 1-2, lines 58-11: Griffin describes executing one or more interim data processing routines at random intervals. In order to execute these routines, the processor must jump from the current

	instruction address to the beginning address of the routine. By randomly varying the time intervals between these jumps and executing the current process, the device is unpredictable, since the definition of random, in relation to computing, is unpredictable. Please see the attached definition for more information.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

38. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
9 November 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100